MTP\_REG\_CRC\_DET IP SPEC

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## Introduction

Check the CRC value of MTP shadow registers every 2ms, if no right, output MTP\_REG\_CRC\_FLT is high.

## Feature

Monitor the MTP shadow register to ensure all values are right.

## Register Definition

### Register Map

Table 1 MTP\_REG\_CRC\_DET Register Map

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Name** | **Add** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **default** |
| FACT\_CRCH | 0x107E | FACT\_CRC16[15:8] | | | | | | | | 0x00 |
| FACT\_CRCL | 0x107F | FACT\_CRC16[7:0] | | | | | | | | 0x00 |
| SYS\_FLT2 | 0x5114 |  |  |  | MTP\_CRC |  |  |  |  | 0x00 |

## Functional Details

### Block Diagram

The following diagram shows the MTP\_REG\_CRC\_DET inputs and outputs.



Figure1 MTP\_REG\_CRC\_DET diagram

### Module input/output list

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Name | Dir | Width | Discirption | duration |
| MTP\_REG\_CRC\_FLT | O | 1 | MTP shadow register crc fault bit | Level(CLK\_SLOW2 domain) |
| CLK\_SLOW2\_SC | I | 1 | Redundant CLK\_SLOW | 256KHz, 50%duty |
| resetb\_SR\_CLK\_SLOW | I | 1 | Scan\_muxed resetb and soft resetb for CLK\_SLOW domain | level |
| load\_done | I | 1 | MTP load done | Level(CLK\_MTP domain) |
| pulse\_SLOW2\_2ms | I | 1 | 2ms pulse in CLK\_SLOW2 domain | 1 CLK\_SLOW2 |
| reg1000~107F | I | 8\*128 | MTPuration registers 1000~107F  (MTP shadow registers) | Level(CLK\_REG domain) |

### Clock Domain

The clock for MTP\_REG\_CRC\_DET is CLK\_SLOW2\_SC.

### MTP\_REG\_CRC\_DET function description

IBM algorithm with polynomial (x16+x15+x2+1) and default value 16’hFFFF is used for CRC. MTP\_adr[6:0] is defined that goes through all MTP shadow registers, i.e., 16’h1000~107F.

MTP\_CRC\_data[7:0] changes to corresponding register value every time MTP\_adr changes.

CRC calculator updates every time MTP\_data[7:0] changes. Once MTP\_adr[6:0] went through all the registers, check the calculator result, if not 0, MTP\_REG\_CRC\_FLT is high.

(HWSR001\_MTP\_REG\_CRC\_DET)